

Amendments to the Specification

Please amend the paragraph appearing at page 12, lines 15, through page 13, line 11, as follows:

Thus in Figure 5(a) a first layer of low k insulating material 10 is deposited on a substrate 11 and a via is part etched in the surface of that material as indicated at 12. At this time the etching of the via formation ~~[[11]]~~ 12 is relatively straightforward because the whole surface of the layer 10 is exposed. In Figure 5(b) a second conformal layer 13 is deposited so that it fills the formation 12 but this formation is then reflected at the surface of the layer 13 as shown at 14. The upper surface of 13 is then masked with the desired wiring pattern and Figure 5(c) shows the part etching of the wiring channel 15. Simultaneously and inevitably the bottom of the formation 14 is also etched and so this progresses down into the formation 12 as shown at (c) and (d). At the point shown in (d) there will be a distance x left to etch in the layer 13, whereas there will be a distance y left to etch in the layer ~~[[11]]~~ 10. Although not clearly shown in the schematic drawings y will usually be greater than x and the ration y/x will determine the relative etch rates which should be selected for the materials of the layers 13 and ~~[[11]]~~ 10. IN the kind of arrangement illustrated in the figures, it is likely that in fact that y will approximately be twice x and so the etch rate of material ~~[[11]]~~ 10 should be twice that of material 13.